

Atty Docket No. 020408-002000US

PTO FAX NO.: (703) 872-9317

ATTENTION: Examiner Justin P. Bettendorf
TELEPHONE NO.: (703) 308-2780

Group Art Unit 2817

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FOR THE PERSONAL ATTENTION OF
EXAMINER JUSTIN P. BETTENDORF

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Document(s) Attached

1. Transmittal Form (1 p)
2. Request for Reconsideration Under 37 CFR 1.116 Expedited Procedure
Examining Group 2817 (4 pp)
3. This Facsimile Transmittal Form (1 p)

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Dated: 02/10/03 *Eleanor J. Taylor*

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| TRANSMITTAL FORM (to be used for all correspondence after initial filing) | Application Number | 09/837,897 | |
| | Filing Date | April 18, 2001 | |
| | First Named Inventor | Allott, Stephen | |
| | Group Art Unit | 2817 | |
| | Examiner Name | Justin P. Bettendorf | |
| Total Number of Pages in This Submission | 1 | Attorney Docket Number | 020408-002000US |

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| Firm and individual name | Townsend and Townsend and Crew LLP Henry K. Woodward | |
| | Reg. No. 22,672 | |
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REQUEST FOR RECONSIDERATION
UNDER 37 CFR 1.116 EXPEDITED
PROCEDURE - EXAMINING GROUP
2817

TOWNSEND and TOWNSEND and CREW LLP

By: Eleanor J. Taylor

PATENT
Attorney Docket No.: 020408-002000US
Client Ref. No.: PN019-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Stephen Allott

Application No.: 09/837,897

Filed: April 18, 2001

For: TRANSCONDUCTANCE DEVICE
EMPLOYING NATIVE MOS
TRANSISTORS

Examiner: Justin P. Bettendorf

REQUEST FOR RECONSIDERATION
UNDER 37 CFR 1.116 EXPEDITED
PROCEDURE EXAMINING GROUP 2817

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Reconsideration is respectfully requested for the Office Action mailed January 7, 2003, finally rejecting claims 1-17 in the above-identified patent application under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figures 1-4 and description thereof in view of Brahmhatt 4,442,481 for reasons of record in the first Office Action, the Examiner alleging that Brahmhatt teaches that native MOSFETS are art recognized equivalent to enhancement mode MOSFETS but have a very low threshold voltage. The Examiner has concluded that substituting alleged art-recognized equivalent native MOSFETS as taught by Brahmhatt in place of generic MOSFETS in the transconductance cell of Applicant's Figure 4 would be a mere substitution of art recognized equivalent MOSFETS.

The Examiner refers to MPEP section 2144.06 that "a suggestion to substitute one equivalent component or process for another is not necessary to render

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substitution obvious." The Examiner further refers to *ex parte* Obiaya, 227 U.S.P.Q. 58, 60 (Board of Appeals and Interferences 1985).

This final rejection is respectfully believed to be in error. First, it will be noted that MPEP 2144.06 in referring to *in re* Ruff states that equivalency cannot be based on the mere fact that components at issue are functional or mechanical equivalents. The decision notes that components which are functionally or mechanically equivalent are not necessarily obvious in view of one another.

Moreover, it is respectfully submitted the native transistors and conventional doped channel transistors are not functionally equivalent, as will be discussed below.

In the present claims, the prior art recognition of using conventional CMOS transistors having p-doped channel regions and n-doped channel regions is not functionally equivalent to the use of native transistors. Indeed, the use of native transistors in a transconductance element or cell for use in a telecommunications receiver system on a chip is not functionally equivalent to using conventional MOS transistors as taught in the prior art, such as disclosed by Johns and Martin, Analog-Integrated Circuit Design, of record in the application. Applicant has recognized a problem with the use of the known transconductance cell due to the adverse effects of source-bulk voltage (VSB) on MOS transistors used in the transconductance cell. Further, control voltage in a gyrator can have a limited dynamic range when using the conventional MOS transistors.

Native transistors have undoped channels and are not equivalent to conventional MOS transistors (CMOS, p-channel, or n-channel) in that the native MOS transistor has a lower threshold voltage V_t which leads to a lower variation of transconductance elements (GM) in a gyrator due to source to bulk voltage variations.

As noted on page four of the specification, the use of a low to zero threshold voltage transistor, a "native" device, improves filter performance in the presence of substrate noise. This is described on page 5 of the specification with reference to Figs. 7A-7B.

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Further, another advantage of using the native MOS transistor is that the control voltage has more dynamic range, as illustrated in Figs. 8A-8D and as described on page 5 of the specification. Further, the native MOS device has a lower transconductance gain with respect to the transconductance control voltage V_c , thus resulting in less jitter of a phase lock loop used to tune a filter, and hence a more stable loop control voltage. Thus a signal processing system on a chip fabricated with transconductance devices employing native MOS transistors can have more accurately controlled cut-off frequencies with reduced substrate noise susceptibility via the VSB voltage.

The transconductance cell for use in a telecommunications receiver system on the chip defined by claims 1-10 and the gyrator as defined by claims 14-17 specifically call out a variable resistance interconnecting nodes of load resistors, the variable transistor resistance comprising a pair of native MOS transistors having low threshold voltage, as illustrated in Figs. 4 and 9 of the drawing.

Further, the method of reducing noise susceptibility due to bulk semiconductor voltage in a system on chip employing gyrators in filter elements as defined by claims 11-13 specifically calls out providing a gyrator cell with resistive loads for a plurality of current sources, the resistive loads including first and second MOS transistors, and connecting a variable resistance between the first and second MOS transistors, the variable resistance comprising two serially connected native MOS transistors having low threshold voltages.

Thus the invention as defined by the claims specifically calls out the use of native MOS transistors, which as described above and disclosed in Applicant's specification offer distinct advantages over the conventional MOS transistors. The use of native MOS transistors in place of the conventional doped channel transistors is obviously not substituting equivalence known for the same purpose as required in MPEP 2144.06. The use of the native transistors offers distinct advantages not recognized in the prior art and overcomes problems in a gyrator associated with adverse effects of source-bulk voltage on MOS transistors. This recognition by Applicant, heretofore unknown in

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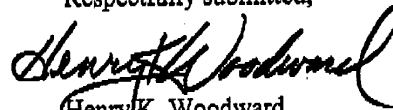
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the prior art, is respectfully believed to be an advancement in the art and a patentable invention.

For the foregoing reasons, it is respectfully submitted that claims 1-17 are patentable under 35 U.S.C. 103(a) over the prior art figures 1-4 in view of Brahmabhatt, and allowance of claims 1-17 is respectfully requested.

Should the Examiner have any questions concerning the present Request for Reconsideration, a telephone call to the undersigned attorney is requested.

Respectfully submitted,


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